Generator Modeling for Analog Emulation of Large Scale Power Systems

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ABSTRACT
Generator Modeling for Analog Emulation of Large Scale Power Systems
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This thesis proposes an approach to modeling generators for solving large-scale power systems in analog emulation. Analog emulation is becoming a computational alternative for power system analysis without the disadvantages of traditional digital computation methods. This approach allows for fast computation independent of system size and the development of accurate models. Circuit modeling and design issues of analog hardware are presented. The proposed generator model will focus on a second order circuit with suggestions for more advanced models. The design is capable of reconfiguring system parameters and emulating load flow calculations with other circuits, i.e. transmission lines and loads. This research focuses generator modeling and its steady-state solutions in traditional load flow studies.
1. INTRODUCTION

1.1. Overview

This thesis examines the realization of generator models for the implementation of analog emulation of large-scale power systems. Analog computation of power networks has been reintroduced as a continuing field of research, due to many technological advances in analog electronics during recent years. This application of analog computation is particularly designed for power systems with the advantage of utilizing faster than real time computation, which is independent of system size.

Currently in the power industry, static load flow analysis is based on the power flow equations. These analyses use a sequential method, which make the simulation process very slow in complex networks and is greatly dependent on the size of the power system network. Digital simulations are becoming more increasingly time intensive as power systems become larger and more complex. Given this, traditional digital simulations use assumptions and simplified models to perform load flow analysis. For this reason, analog computation is becoming a feasible alternative solution for power system analysis.

Without suitable models of power system components, analog computation cannot truly be realized. Even though digital methods are very precise, the models are usually simplified to reduce the simulation time, whereas detailed analog models can be developed and implemented without any significant effect on the emulation time. The main concern regarding the design and modeling of analog generator models presented in the thesis include the computation speedup of valid model solutions.
The work provided in this thesis is just a portion of the ongoing research endeavor to develop a Power System on a Chip (PSoC) [1, 2]. Concentration in this thesis will only focus only on the generator, although other devices also being studied including transmission lines [3], loads [4], and tap-changing transformers. In order to accomplish the end goal of a PSoC, a simplified illustration of developmental stages [5] is presented in Figure 1.

Figure 1: PSoC Development Stages [5]

The development process of the PSoC involves four stages including feasibility studies, Printed Circuit Board (PCB) design, Very Large-Scale Integration (VLSI) design, and VLSI implementation. Stage I concentrates on the concept validation of analog computation as a tool for power system studies. This is demonstrated with Analog Behavior Modeling (ABM) of electric circuits in PSpice that represents the power system
and its behavior. This stage describes the intricacies of circuit connections and allows for model validation without any full structural circuit design.

Stage II realizes the verified analog behavior models and develops analog circuitry to replace the building blocks assembled in the previous stage. Using CMOS devices and software packages, the design, simulation, and PCB layout of power system components, i.e. generators, loads, transmission lines, etc, can be achieved. This development stage is broken up into two parts entailing circuit modeling and simulation and PC board development and emulation. This stage is the primary focus of this thesis.

The last two Stages III and IV transfer this circuit realization into a VLSI design and the final fabrication of a “Power System on a Chip”. Many of the issues that will be addressed in Stage II will be similar to issues in the VLSI stages. With these issues recognized and addressed in the previous stage, the final stages can be designed with these issues known beforehand. These include modeling realizations of various power system components in addition to control and data acquisition schemes. The standout issue in these stages will be scalability issues involving system size capability and associated ramifications. The goal being to qualify and quantify what size power system can be captured on a given VLSI chip.

The next section details the background and history of analog emulators and digital simulators of power system studies. Difference between the two types of computational methods will be examined as well as technology advances that have occurred to renew interest in analog computation.
1.2. Background

The difference between emulation and simulation is sometimes vague and the two can be confused due to their common functions. Here, an emulator mimics a specific system and is capable of achieving the same results and behaviors as the original system, whereas a simulator represents the system using approximate behaviors or simplified models. Typically, simulations are accomplished using digital computers, while emulations with analogue computers.

Even though the first analogue computers where purely mechanical computers [6], the advent of electrical computers overcame the issue of low speed solution of differential equations in mechanical computers. With electrical computers developed, power system computation originally started in the 1920’s using AC Network Analyzers to model and solve problems associated with power distribution systems [7].

These special-purpose analyzers were essentially scaled models of a power system. Some manufacturers of electronic analog computers included Applied Dynamics Inc., Burr-Brown Research Corporation, Comcor Inc., General Electric Company, and Hitachi Ltd. The electrical analog computer is an analogy of the physical system, hence its name. The computers could represent the electrical equivalent using power supplies, operational amplifiers (op-amps) and could control parameters using potentiometers. The analog computer was very popular until the development of the digital computer.

Unlike analogue computers, digital computers have the advantage of very precise calculations using an iterative computational process, though at the cost of longer simulation times. Digital computers did not become prevalent in power system studies until the middle of the 20th century. One of the first applications was the digital computer
being used to solve a power system load flow problem [8]. With the ability to solve complex system with high degree of precision, smaller computer size, cost, and maintenance, the digital computer began to replace the large and expensive analogue computers.

Another example of an analog computer is the special-purpose hybrid computer. A hybrid computer consists of an analog computer that would provide quick but imprecise initial conditions to a digital computer for more precise solution. With the development of analog-to-digital (A/D) and digital-to-analog (D/A) converters, hybrid computers were used to solve many applications in power systems [9].

An example of the size of an analogue hybrid computer can be seen in Figure 2. The computing system shown was introduced in 1964 by Applied Dynamics [10]. The model AD-256 consisted of 256 amplifiers, comprising of 48 integrators, 80 summers, and 128 inverters. It had an operational range of ±100 volts DC and 200 coefficient potentiometers for carrying system parameters.
With a large number of power system problems that are more conveniently and economically solved on an analog hybrid computer [9], this research is geared towards revisiting past analog/hybrid computation techniques and utilizing them today with current semiconductor technology. In the past two decades, silicon-on-insulator complementary metal oxide semiconductor (SOI CMOS) technology has become a major technology for integrating VLSI systems using a low-supply voltage [11, 12]. Along with the progress in the CMOS technology, CMOS devices have been scaled down continuously and the corresponding power consumption has been decreased, which have triggered advances in the circuit design techniques for various designs and applications previously unattainable.

For the reason that the association between CMOS circuits and VLSI chips is becoming increasingly easier to implement, designing a small analog computer for power system analysis has now become feasible. Therefore, the old analog computers and network analyzers that were very large and especially complicated to reconfigure, a novel equivalent can be fabricated on a relatively small VLSI chip wafer and be reconfigured from a digital computer using A/D and D/A converters.

1.3. Problem Statement and Motivation

In today’s “Information Age”, the world’s reliance on electricity has become a costly one. Since electric power has become an indispensable commodity, engineers are faced with the difficult task and responsibility of providing electricity to customers using arguably the largest and most complex man-made machine on the planet. To avoid interruptions and outages, careful planning and operation of the power system network is required to provide safe, reliable power to other important infrastructures and services
like water, telephones, transportation, hospitals, and the like. Depending on which source is used, it is estimated that the loss of power costs the economy anywhere between twenty to one hundred twenty billions dollars a year [13].

Even though the power system overall is very reliable, the system is still susceptible to power outages and even the smallest outages cost consumers money. One study published in 2004 by Ernest Orlando Lawrence Berkeley National Laboratory assessed that power outages in the United States result in a monetary losses of an estimated eighty billion dollars annually [13], based on the best information available in the public domain.

Although major blackouts and downtimes are most evident because they occur less frequent, short-term momentary outages, which last 5 minutes or less than 5 minutes and occur more frequent, have a stronger impact on the total cost of interruptions than sustained interruptions. This is represented in Figure 3, which also illustrates that majority of the monetary cost of outages are endured by the commercial and industrial areas, and not the residential. Some companies are so vulnerable to power outages, that they build redundant feeds from multiple power sources to minimize downtime due to interruptions.

![Figure 3: Base-Case Estimate of the Cost of Power Interruptions [13]](image)
The blackout of August 14, 2003 [14] showed that the electric power grid is capable of catastrophic interruptions, with some calling the current state of the power grid antiquated. One solution to improve the reliability of the power grid, albeit a costly one, would be to upgrade and replace much of the infrastructure with modernized equipment. The maintenance and upgrading of the current infrastructure is a slow expensive process. An alternative solution to improving reliability would be to improve power system operation, an important aspect in power systems. Better decisions can be made for power system reliability, if the power system operators have better information.

Based on this information, power outages are very expensive for business operations. Along with the deregulation of the electric power industry, maintaining the quality and reliability of the power grid on a daily basis has become very challenging. Currently, Regional Transmission Organizations (RTOs) have a fix amount of time daily to perform fault analysis (contingencies) and economic analysis (day ahead) for each market area [15]. If their network size increases because they now monitor a larger area, the computational time will increase but not the allotted time for analysis. This will limit the number of contingencies studied and provide less comprehensive economic analysis. This is where faster computation can improve overall system analysis and lead to improved system security and reliability.

The advantage of analog emulation over current digital methods is the computational speed through its true parallel nature. This application of an analog power system computer has the potential to become a real-time or faster than real time computational tool for large complex power networks. With faster computation, analysis that is more detailed and complete can be attained. This would result in better planning
and operation by engineers during critical times, which will ultimately lead to fewer power interruptions. Faster computational tools, analog emulation in this case, need to be developed to help prevent system downtime and make the electric power grid safer, more secure, and more reliable. With such a large economic impact on the society, the need for research into faster computational tools is necessary.

1.4. Organization of Thesis

This thesis is arranged in a manner to present the research clearly. The software used for the design and testing development stages and the benchmarking of results are discussed in Chapter 2. Chapter 3 provides a brief summary of generator modeling and describes the proposed generator model and the underlying assumptions made. The overview of analog emulation of power systems and the representation of the generator model will be described in Chapter 4. Chapter 5 introduces the analog devices used, the rationale behind their selection, and the analog circuits representing the proposed analog generator module. The software validation and hardware testing of the analog circuits are illustrated in Chapter 6, followed by the conclusion, summary of work, and recommendation for future work given in Chapter 7.
2. DESIGN AND BENCHMARKING ENVIRONMENT

2.1. Overview

This thesis presents the formulation and realization of generator modeling for the purpose of analog emulation of large-scale power systems. In order to construct an analog generator model, many development tools are required. Software (SW) and hardware (HW) tools alike were utilized to aid in the design process, test the analog functionality, and verify the results as power flow solutions. A feasibility study was previously conducted [5] using Analog Behaviors Models (ABMs) within a PSpice design environment. This approach was capable of validating the core components and computational methods that are to be used in the analog emulator. This work focuses on replacing the analog behavior models, which are based on mathematical equations, and replace them with equivalent analog circuitry.

2.2. PSpice

Since this research involves analog circuitry, an advanced simulation tool for mixed-signal and analog environments is needed. PSpice is a general-purpose analog circuit simulator, more specially a PC Simulation Program with Integrated Circuits Emphasis (PSPICE). It is used extensively throughout this thesis to check the integrity of circuit designs, while predicting the circuit behavior. It is a common tool in Electronic Design Automation (EDA) for the designing and producing of electronic systems ranging from printed circuit boards (PCBs) to integrated circuits (ICs).

The software used specifically in this thesis is Cadence PSD 15.1 [16], which is a commercially available package that includes OrCAD Capture CIS 10.1 [17] and PSpice
A/D [18]. Capture CIS provides an intuitive graphical interface to the schematic design, which includes part libraries, part and property editors, and hierarchy design for subcircuit reuse. Another advantage of this software package is the capability to create netlists that are used by PSpice for circuit simulation or Layout for PCB design. This application can be seen in Figure 4 with an Operational Amplifier (op-amp) in an inverting amplifier configuration. Voltages probes are used to monitor the input and output voltages of the circuit.

![Figure 4: Circuit Schematic with Probes in Capture](image)

Once the circuit design is entered into Capture, the advanced capabilities of PSpice simulation can be used for accurate analog and mixed-signal solutions. Simulations can be performed by transient analysis, ac/dc sweep analysis, parametric
sweep, Monte Carlo analysis, etc. PSpice uses macro-models to mimic the response of the actual devices. Figure 5 represents the voltage probes seen in Figure 4, plotting the input and output voltages of the inverting amplifier circuit, along with the transfer function. PSpice allows the designer to visualize the expected results, which can be used to verify and validate circuit designs.

Note that macro-models are intended as an aide in the design and prototyping of analog circuits. Simulations including these models are not substitutes for the actual devices, but act as a supplement to the hardware testing of the devices. The models and information provided within, are rather reliable and correct, but sometimes are expressed as having ideal properties. It is expected that the results provided in this thesis will have some discrepancies between software and hardware analog circuit results, due to some inaccuracies within the provided PSpice models. All results will be compared to ideal solutions and results from industrial load flow programs.
2.3. Benchmarking Tools

Many of the manufacturer models that are used in analog simulation contain assumptions to simplify the device model and characteristics. In order to justify simulated software results and measured hardware results, ideal solutions will be necessary to validate the data. Two methods of benchmarking and validation will be provided throughout this research. First, the accuracy of the analog circuit will be compared to mathematical equivalent using behavioral models. Second, the actual solution(s) of the power system analog emulator will be compared to traditional industry load-flow solvers.

2.3.1. MATLAB/Simulink and PSpice ABM

Analog Behavioral Models, which are a feature within PSpice, can be used to mimic the response of electronic components in terms of mathematical equations or transfer functions within blocks. These building blocks are used together to construct the ideal model of a dynamic system. Simulink [19] is another tool for modeling, simulating and analyzing dynamic systems with the use of mathematical blocks. Both of these programs are capable of running fixed-step or variable-step simulations of time-varying systems. Since based on mathematical equations, the block diagrams represent the input/output relationship of ideal components like integrators, multipliers, adders, etc. This is very useful in verifying the behavior of analog circuit components. Both of these applications will be used interchangeably when validating and comparing results of circuit simulations.
2.3.2. PowerWorld

PowerWorld Simulator [20] is an interactive power simulation package designed to simulate high-voltage power systems visually. Simulator has a number of uses in the corporate and educational environments. Some of these include Power Flow Analysis, Fault Analysis, Economic Analysis, and Locational Marginal Pricing (LMP), to name just a few. Power World Simulator uses a full Newton-Raphson algorithm [21] with non-divergence control, and is capable of efficiently solving systems with up to 100,000 buses. Power systems are graphically represented by a single line diagram consisting of power system components and buses. An example power system in Figure 6 shows a one-line diagram of a seven-bus power system in the PowerWorld interface. Parameters of all components are user adjustable and set to represent their real world counterparts with dialog boxes.

![Figure 6: PowerWorld One-Line Diagram of a 7-Bus Power System](image-url)
This software uses a graphical interface to display the power system and its results. The actual flow of power is displayed in pie chart format representing the limits of each transmission line. Another feature is the ability to separate the power system into regions that can be helpful when performing economic analysis. The PowerWorld test case used in this thesis will consist of two generators, three transmission lines, and 1 load in the three-bus configuration. The results of this simulator are compared directly to the PSpice and hardware results of the analog emulator.

2.4. Hardware

All analog hardware circuits were built with commercially available CMOS components on breadboards. The prototypes built were designed to fit into National Instruments® Signal Conditioning Extension for Instrumentation (SCXI) modules. SCXI provides a modular instrumentation platform for measurement and automated systems. Laboratory Virtual Instrumentation Engineering Workbench (LabVIEW) software provides a development environment using a visual programming dataflow language called G. Using National Instruments® LabVIEW [22] software and data acquisition (DAQ) hardware, the power system prototype is capable of data measurement, actuation/configuration, control, and automation.

The analog generator module will connect to a computer interface using DAQ hardware which includes analog inputs, analog outputs, digital input/output channels, and counter/timers. This allows for full control of the hardware using custom-built LabVIEW Virtual Instruments (VIs) which provides a user interface to the DAQ hardware. Figure 7 represents the emulator hardware setup for a small power system. This illustrates the connection between the analog modules and the computer data acquisition and control.
For the purpose of testing the generator model analog prototype, the setup will include external supplies for power, oscilloscopes to aid in measurement, and computer connections that allows remote control, configuration, and actuation of the generator circuit parameters along with data acquisition from the analog hardware.

Figure 7: IEEE 3-Bus Power System Emulator Hardware Setup
3. POWER SYSTEM GENERATOR MODELING

3.1. Overview

The synchronous generator is one of the most important and widely used power sources throughout the world [23]. Synchronous generators convert mechanical energy into electrical energy, which supplies the complex power to the loads within the electric power system. In this chapter, our interest is the understanding and operation of the generator within a large interconnected electrical power system, with the emphasis on the steady state and transient behavior of the generator. With this knowledge, we can design an appropriate generator model with the main concentration specifically on steady-state load flow analysis.

3.2. Classical Steady-State Model

The voltage that is produced internally to the generator, \( E_a \), is not necessarily the voltage, \( V_a \), that is seen at the output of the generator terminals. The only time that the voltages are equal is when there is no armature current, \( I_a \), flowing in the machine. The classical generator model that will be used in this thesis consists of a voltage source behind an impedance \( Z \), which includes the synchronous reactance, \( X_s \), and the winding resistance, \( R \). Since the armature reactance and the self-inductance of the machine are both represented by a reactance, they are lumped together to define the synchronous reactance of the generator. The relationship between the internal voltage and the terminal voltage is represented by the following equation:

\[
V_a = E_a - I_a R - jI_a X_s
\]  

(3.1)
With the generator voltage affected by the internal resistance and reactance, a simple circuit consisting of a resistor and inductor in series with a voltage source represents the equivalent model of the generator as seen in Figure 8.

\[
Z = R + jX_s
\]

\[
E_a = |E_a| \angle \delta
\]

\[
V_a
\]

Figure 8: Per Phase Equivalent Circuit of a Generator for Steady-State Analysis

In the real world, the synchronous reactance of the generator is typically much larger than the winding resistance, \( R \) [24]. Since this is the case, neglecting the resistance allows for simplified equations that produce comparatively accurate results.

3.3. Classical Transient Model

Since we are concerned about multi-machine stability studies of large power systems, a more appropriate model is the transient reactance behind a voltage source. The previous model included only a saturated reactance, which is only good in steady-state stability. Very similar to the previous model, this transient classical model includes only the direct-axis transient reactance, \( X_d' \), as seen in Figure 9.
This model provides the transient behavior of the generator during and after a fault. It allows the pre-fault conditions to initialize the transient response during and after a fault is cleared, then returns to a steady-state condition. With this dynamic approach, the model can be used for transient stability analysis and steady state representation. Assumptions that are valid with this model include [25]:

- The mechanical power input is constant.
- Damping or asynchronous power is negligible.
- The synchronous generators are represented electrically, by constant voltage behind a transient reactance models.
- The mechanical rotor angle corresponds to the angle of the internal voltage behind the transient reactance.

This model is useful for stability analysis but is limited to the study of transients for only the “first swing” or for short periods on the order of one second [25]. For clarification, $|E_G|$ will represent the internal generator magnitude, as opposed to $|E_a|$. 

![Figure 9: Per Phase Equivalent Circuit of a Generator for Transient Analysis](image)
3.4. Swing Equation Dynamics

For both models presented, the electrical angle, $\delta$, which is the angle between the internal armature voltage and the terminal voltage, is unknown, and therefore needs to be computed. In order to determine the electrical angle, we need to capture the dynamics of the generator within our model. The simplified mechanical equation that governs the motion of the generator rotor, describes the swing between the mechanical and electrical angle, otherwise known as the swing equation,

$$M \ddot{\delta} + D \dot{\delta} + P_e(\delta) = P_m$$  \hspace{1cm} (3.2)

where $M$ is the generator inertia coefficient, $D$ is the damping coefficient, $P_e$ is the electrical power output, and $P_m$ is the mechanical input power. The functional block diagram of the swing equation can be seen in Figure 10, which will provide a layout for the generator model that will be presented in the following section.

![Figure 10: Swing Equation Functional Block Diagram](image)

This model can simplify the complex nature of the non-linear dynamics of the classical generator without significantly reducing the precision of the model by
neglecting damping. Higher order complex generator models are identified to only increase accuracy by 1-2% when adding detailed modifications to the traditional classical model [26]. With these assumptions, the swing equation (3.2) will reduce to only the difference between the mechanical input power and the electrical output power. After factoring in the generator inertia coefficient and taking two integration steps of the angular acceleration, the solution of the electrical power angle can be calculated in the following form.

\[
\delta = \frac{1}{M} \int \int (P_m - P_e(\delta)) \, dt \, dt
\]  

Equation (3.3) represents calculation the electrical angle between the mechanical and electrical power and will provide the main computational engine to the analog generator model.

3.5. Proposed Model

The generator model that will be implemented in analog hardware for this thesis will be a second-order model with reactive power limits, which allows the generator to be active or passive in supporting voltage stability. The model is capable of “first swing” transient analysis, but specifically designed for use in steady-state analysis with terminal fault capabilities.

In order to simplify the calculation required in the analog circuit, the electrical power output of the generator will be solved in rectangular form. By converting the polar notation to rectangular form, only the real and imaginary components will be necessary
and the calculation for the electrical output power of the generator model can be rewritten as the following equation.

\[
Re\{S\} = Re\{V \cdot I^*\}
\]

\[
P_e = E_{\text{Real}} \cdot I_{\text{Real}} + E_{\text{Imag}} \cdot I_{\text{Imag}}
\]

\[
P_e = |E_g| \cdot \cos \delta \cdot Re\{I\} + |E_g| \cdot \sin \delta \cdot Im\{I\}
\]  

(3.4)

The calculation for the electrical output power will be essential to the generator model because this will need to be applied directly into the swing equation (3.3) for the calculation of the electrical angle. For the analog hardware scaling, which will be discussed further in Chapter 4, the power system’s electrical and mechanical power will be represented as current and the electrical angle will be represented as voltage. Applying (3.4) to (3.3), modifies the functional block diagram for the developed generator model, which is shown in Figure 11.

![Figure 11: Generator Model Functional Block Diagram](image)

The generator model will be comprised of two important parts: the calculator, which updates the electrical angle of the generator model, and the generator source,
which provides the electrical power, in rectangular form, to the network. Measuring the output current of the generator and feeding that measurement back into the model to the calculator portion, updates equations (3.3) and (3.4), specifically $P_e(\delta)$, continuously. The reactive power, $Q_e(\delta)$, will be updated for the measured current output of the generator for a specific internal voltage, $|E_G|$, which is controlled via the computer. The model will calculate and monitor the electrical real power output, electrical reactive power output, and the electrical angle. This model will incorporate reactive power (VAR) controller, which will allow the model to have the capability of being a constant power and voltage (PV) generator or a constant power and reactive power (PQ) generator. Currently the VAR limit controller can be modeled externally within the computer control as shown in Figure 12.

![Figure 12: Detailed Block Diagram of Proposed Generator Model](image-url)
3.6. Advanced Modeling

The advantage to the functional block diagram modeling of the generator is its flexibility. Building higher-order and more complex models is achieved through the addition of extra controllers in various feedback loops. Future development of an advanced generator could incorporate various elements like a governor, an exciter, and damping as seen by Figure 13.

![Figure 13: Advanced Generator Model Block Diagram](image)

Figure 13 represents the function block diagram of the swing equation (3.2) that represents the analog generator circuit. This shows a classical generator model that includes second-order dynamics and damping. The control of a switch enables the
creation of a fault to study the transient behavior of the model. Using analog adders, multipliers, integrators, trigonometric functions, etc, many complex generator models can be created with analog components. For example, to incorporate a governor within the model, a simple feedback loop after the first integrator would send $\omega$ to the governor model, comparing it to $\omega_{ref}$ to control the input mechanical power, $P_m$. In addition, if an exciter model was desired, feeding back the network currents and the generator terminal voltages to a feedback control, which would determine $E_{fd}$ to maintain voltage output. A controller would be used to determine if the model was solving steady state or transient solutions. This would allow the addition of VAR limit control on the output of a steady-state generator model. This illustrates that the basic structure will still be maintained if they were to be incorporated.

The generator models presented here are the basis for the analog generator circuit modeling for steady state power flow analysis in this thesis. Analog circuit equivalents to the block diagrams used are derived, developed, and tested for the analog power flow emulation. Chapter 4 details this analog computational method and the modeling of power system components with emphasis on the generator for this application.
4. METHODOLOGY AND DEVELOPMENT OF ANALOG EMULATION

4.1. Introduction

This chapter presents the fundamental theory behind this analog computational approach and each power system component is identified separately. Various approaches for analog computation of power flow have been previously introduced. More specifically, this thesis uses one approach first developed by Fried et al [27], which uses a DC emulation technique that preserves the original power system network topology and provides a fully integrated solution.

4.2. Overview of Analog Emulation of Power System

For the DC emulation method used in this thesis, a general classical power system model in Figure 14 is utilized and contains three main components: generators, transmission lines, and loads.

Figure 14: General Classical Model of a Power System Network [27]
The transmission network is modeled by a set of buses or nodes interconnected by transmission links. Generators and loads that are connected to various buses of the system inject and remove power from the transmission network, respectively. Figure 15 illustrates how the power system components will be interconnected and what type of models will be discussed in Section 4.3.

In this technique, the complete power system grid to be emulated (including every generator, transmission line, transformer, and load) is transformed and decomposed into several low voltage, low current DC circuits that are mapped directly onto a VLSI chip. Therefore, a complete circuit representation of the power grid is placed in a single mixed-signal VLSI microchip. This technique allows the simulation to be performed completely in DC, where all the transformed network components are frequency independent.

Typically, in digital power system computation, the states and parameters of the power system are realized in polar coordinates, i.e. in the form of the magnitude and angle of the state and parameter. In the DC emulation approach of power systems, Cartesian (or rectangular) coordinates are also used for computation, with conversion to
and from polar coordinates conducted at different stages of the analog calculator. Figure 16 represents the coordinate transformation of polar coordinates and Cartesian coordinates on a complex plane.

Figure 16: Coordinate Transformation

The polar representation of a vector comprises of two components, a magnitude and phase, which is represented in the following manner.

\[ V = |V| \angle \theta \quad (4.1) \]

The Cartesian or rectangular form of the polar expression consists of two parts, a real component and an imaginary component, which is represented in the following manner using Euler’s formula.

\[ V = V_{\text{real}} + jV_{\text{imag}} = |V| \cos \theta + j|V| \sin \theta \quad (4.2) \]
This DC emulation approach was previously proposed and discussed in [27]. This approach uses nodal analysis on the power system network, where power system voltages applied to the network admittances determine the injected currents at the nodes.

\[
I = Y \cdot V
\]

\[
(I_{re} + jI_{im}) = (V_{re}Y_{re} + jV_{im}Y_{im})
\]

\[
= (V_{re}Y_{re} - V_{im}Y_{im}) + j(V_{re}Y_{im} + V_{im}Y_{re})
\]

\[
= V_{re}Y_{re} - V_{im}Y_{im} + jV_{re}Y_{im} + jV_{im}Y_{re}
\]

The computation of the complex current flow through any given branch or transmission line is a direct result of the relation between the real and imaginary voltages at a node or bus and the transmission line admittance. This DC emulation approach requires four separate dc resistive networks to calculate the complex current. The real component of the current, \(I_{re}\), comprises of the summation of \(V_{re}Y_{re}\) (Network 1) and \(-V_{im}Y_{im}\) (Network 2) and the imaginary component of the current, \(I_{im}\), comprises of the summation of \(jV_{re}Y_{im}\) (Network 3) and \(jV_{im}Y_{re}\) (Network 4). The resistors represent the network admittance, with the assumption that the angular frequency is relatively constant including only small perturbations within 1-2%. With control equipment and automatic voltage regulators (AVR) implemented in today’s power system, this is a realistic assumption. The real and imaginary admittance parameters are scaled to dc resistor values and using programmable resistors can account for different line parameters.

In this thesis, the generator is modeled as a PV (real power and fixed voltage) regulated generator, which provides the bus voltage and current injection, the transmission line is modeled as a short transmission line with parameters represented by
four passive resistive networks, and the loads will be modeled as constant current sinks.

The following section will describe each component in detail.

4.3. Power System Emulation Components

This section summarizes the power system components that are used in the emulation of load flow computation. The power system model will focus on the three most important elements, the generators, transmission lines, and loads. Each component is designed separately as a modular component, where a large-scale real-world power system can be built with any number of components and configured with real power system parameters. The implementation in this thesis will focus on the analog circuit of the generator that could be easily adapted to a final PSoC VLSI design.

4.3.1. Generators

A generator produces electrical energy from a mechanical energy source. The work in this thesis will focus on the second-order classical generator model that was proposed in Section 3.5. The generator model represents the relationship between the mechanical and electrical power. The solution of the swing equation (3.3) represents the electrical power angle from the difference between the mechanical and electrical power, at any time. This angle along with the appropriate internal generator voltage, are used to determine the real and imaginary terminal voltages applied to the DC emulation admittance network, in rectangular coordinates. This is discussed in more detail in the following Chapter 5.

The advantage of the model used in this thesis, as described in Chapter 3, is that it can be used as a building block to design simple or complex generator models that
computationally represent many types of power system generators. This includes generators with or without varying types and/or levels of control e.g. AVRs, governor controls, excitation systems, etc.

4.3.2. Transmission Lines

Transmission lines represent the power system network, commonly referred to as the grid, because of its interconnected nature that transfers electrical power from one location, sending end, to another location, receiving end. There are three common lumped parameter transmission line models for varying lengths, \( l \); the short-line model \((l < 50 \text{ miles})\), the medium-line model \((50 \text{ miles} < l < 150 \text{ miles})\), and the long-line model \((l > 150 \text{ miles})\) \cite{23}. Concentrating on the short transmission line in Figure 17, the model is represented by lumped parameters resistance, \( R \), and inductance, \( L \), and can be depicted with a lossy model that includes resistance, \( R \) or a lossless model, which neglects the resistance.

![Figure 17: Model of a Short Transmission Line](image)
In the short-line model, the shunt admittance of the transmission line is neglected because the effect of capacitance is minimal for short distances. This type of line is modeled by the series impedance defined as

\[ Z = R + jX_L \] (4.4)

from which the series admittance of the line from node \( i \) to node \( j \) for lossless and lossy models is defined as the following.

\[
Y_{ij,LOSSLESS} = \frac{1}{jX_{Lij}}
\]

\[
Y_{ij,LOSSY} = \frac{1}{R_j + jX_{Lij}}
\] (4.5)

With DC emulation, the transmission lines are required to use real and imaginary resistor components. The sizing of the resistor is dependent upon the resistance and reactance of the transmission line. The transformation of the transmission line’s complex admittance to its resistance value for the real and imaginary part of the DC networks is through complex conjugation as seen below [27].

\[
R_{Re\{Y\}} = \frac{1}{Re\{Y_j\}} = \frac{R_j^2 + X_{Lij}^2}{R_j}
\]

\[
R_{Im\{Y\}} = \frac{1}{Im\{Y_j\}} = \frac{R_j^2 - X_{Lij}^2}{X_{Lij}}
\] (4.6)
4.3.3. Loads

A load model is a mathematical representation of the relationship between the power or current consumed by the load bus and the voltage at that bus. The main function of loads is to sink or source current as needed from the power system network. This thesis assumes that the response of the load to voltage changes is fast and the steady-state solution of the load is found almost instantaneously, which reflects the behavior of a static load model. There are many static load models for power system studies [28] including constant power, $S_P$, constant current, $S_I$, constant impedance, $S_Z$, and polynomial, $S_{ZIP}$.

Constant power loads represent the real and reactive powers consumed at the load bus of the power system and are independent of the bus voltage magnitude.

\[ S_P = P_{Load} + jQ_{Load} \quad (4.7) \]

Constant current loads characterize the real and reactive powers consumed at the load bus that vary directly with the voltage magnitude at the load bus.

\[ S_I = V_{Load} \cdot I^*_{Load} \quad (4.8) \]

Constant impedance loads imitate a nonlinear load model, where the real and reactive powers vary directly with the square of the voltage magnitude at the load bus.

\[ S_Z = \frac{V^2_{Load}}{Z^*_{Load}} \quad (4.9) \]
Polynomial loads correspond to a nonlinear load model with the active and reactive powers described as a linear combination of the three above-mentioned load models,

\[ S_{ZIP} = \alpha_1 \cdot S_p + \alpha_2 \cdot S_i + \alpha_3 \cdot S_Z \]

\[ I = \alpha_1 + \alpha_2 + \alpha_3 \]  

where, \( \alpha_i \) are constant parameters of the load models, summing up to one. These parameters designate how the nominal power is divided into constant power, constant current and constant impedance loads.

Since the focus of this thesis is on the development of generator modeling for analog emulation, this thesis will only utilize the constant current load in all power system examples. The circuit realization of the load model is similar to the generator model, which is discussed in Chapter 5.

4.4. Scaling Parameters

A key aspect to the analog emulator that increases its flexibility is the use of scaling factors. The scaling factors are constants that correlate the real world power system parameters and variables to the parameters and variables of the analog emulator. The selection of proper scaling factors are essential because if inherent consideration of physical operating constraints of the emulator. Two important scaling parameters are due to magnitude and time. Further details on methods and considerations on selection of scale can be found in [29]. In addition, another key factor discussed in this section includes the scaling of parameter space.
4.4.1. Magnitude Scaling

Magnitude scaling consists of various parameters that convert the physical real world power system quantities to the analog emulator circuit quantities and vice versa. This can be considered a two-step process, first involving the normalization of the power system quantities to a per-unit (p.u.) system, and then scaling the p.u. power system to levels appropriate for low-power analog circuits.

\[
\text{per-unit value} = \frac{\text{quantity in standard units}}{\text{base value}} \quad (4.11)
\]

The per-unit scaling normalizes the power system to common base reference values. This allows for numerically robust solution of the power system equations and shows the parameters as a percentage of the base value. Common base values include \( S_b \), \( V_b \), \( I_b \), and \( Z_b \), and conform to Ohm’s law. For this thesis, base values for power, \( S_b \), and voltage, \( V_b \), will be selected and all other base values are derived from these. The per-unit value is related to the base value in the following manner.
Very similar to this process is the next step involving the circuit scaling. To scale the magnitude of the power system to emulator quantities, we use

\[
X \cdot \frac{X_k}{X_b} = x
\]

(4.12)

where,

- \(X\) is the quantity of the physical power system in standard units,
- \(X_k\) is the base value of the analog emulator,
- \(X_b\) is the base value of the power system,
- \(x\) is the quantity of the emulator in standard units.

This scale factor also includes \(S_k, V_k, I_k,\) and \(Z_k,\) and conform to Ohm’s law. For this thesis, the values of voltage, \(V_k,\) and impedance, \(Z_k,\) will be selected and the remaining values derived from the voltage and impedance by the natural laws of electrical circuits. This circuit scaling is the reverse of the normalization of the power system, because it takes the per-unit value from a base reference value and converts it into actual allowable quantities for the low-power electrical circuits of the analog emulator.

4.4.2. Time Scaling

The time scale factor, \(\tau,\) is a constant that represents a computational speedup of \(\tau\) times faster than the real-time system. This factor is directly proportional to the real time of the power system, \(t,\) for a given simulation time of the analog emulator, \(T.\)
This factor always allows the emulator to be $\tau$ times faster or slower than any given power system. The advantage of this time scaling allows the emulator to provide faster than real-time solutions needed for quick decisions or contingency analysis, or provide real-time solutions that could be used as a training simulator for power system operators. The time scale factor is included in the solution of the electrical angle (3.3) in the following manner.

$$\delta = \tau^2 \frac{1}{M} \int \int \left( P_m - P_e(\delta) \right) dt \, dt$$  \hspace{1cm} (4.14)$$

The time scale factor needs to be squared because of the second-order nature involved in the dynamics of the classical generator model. A corroborating factor that may influence the choice of the time scale is that the error in the integration may be accentuated by long emulation times.

4.4.3. Parameter Space Scaling

In parameter space scaling, there are $\delta \rightarrow V$ and $P \rightarrow I$ transformations. These transformations are necessary for the proposed generator model. As described in Section 3.5, two major components are connected within the generator module. The first component is the internal calculator circuit representing the swing equation and the second is the physical electrical circuit representing the actual interconnection with the power system network. This parameter space scaling is essential for the internal
calculator circuit, which intrinsically associates the real world generator to the analog circuit generator.

The first scaling procedure that needs to be addressed is parameter scaling of the electrical angle to voltage. This introduces the desired voltage, \( \nu \), to be represented as a voltage level in the emulator that is equivalent to \( \pi \) radians, and (4.14) can be rewritten as the following equation.

\[
\delta = \frac{\tau^2}{M} \frac{\nu}{\pi} \int \left( P_m - P_e(\delta) \right) dt dt
\] (4.15)

To simplify the circuit, Kirchhoff’s current law will be used to calculate the difference between the mechanical and electrical power in the generator model. In order to achieve this, the power in the circuit needs to be represented as a current. The power-to-current transformation, \( P \rightarrow I \), is only required for the calculation involved within the swing equation (3.2), meaning that the output power of the generator supplied to the network will be measured from the voltage and current outputs at the generator terminals. The conversion of power system parameters to circuit parameters is determined by the selection of circuit magnitude scaling parameters, described in Section 4.4.1, and allows the rewrite of equation (4.15) in terms of voltages and currents.

\[
(\nu \equiv \delta) = \frac{\tau^2}{M} \frac{\nu}{\pi} \int \left( I_m - I_e(\nu) \right) dt dt
\] (4.16)

With the generator model and scaling parameters defined, we can proceed to develop an analog generator model using CMOS analog devices. When selecting the
devices, we need to identify the circuit parameters needed to scale the power system to an analog circuit and the parameters needed to achieve reconfigurability within the model. This is all outlined in Chapter 5, along with other necessary CMOS devices, followed by examples that the generator model will be used. Chapter 6 will verify the design of the analog generator model by providing tests and results of the examples given.
5. METHODOLOGY AND DEVELOPMENT OF ANALOG GENERATOR MODELS

5.1. Introduction

Chapter 3 summarized different generator models for use in an analog emulator, with Chapter 4 describing the behavior and scaling of the DC emulation technique used for power flow analysis. Keeping in mind the advantages of analog emulation and the scaling of power system to analog circuitry, the hardware model is intended to have certain characteristics such as system reconfigurability for a single hardware design, high accuracy, low cost using commercially available off-the-shelf (COTS) parts, and easy transition to VLSI for large-scale capability.

This chapter addresses the concept of reconfigurability in the generator model, along with low cost CMOS parts, high accuracy, and device offsets. Reconfiguration will allow for the change of the system parameters for a given hardware design via external control signals. The control signals actuate the circuit parameters and configure the analog generator module as opposed to the concept of adaptability, which involves model parameters adapting to changing conditions. To accomplish this, the actual analog circuit representing the generator needs to incorporate a programmable analog device into the model to obtain controllable behaviors of the power system. Specifically, the active analog component chosen that realizes these key features is the Operational Transconductance Amplifier (OTA).
5.2. Device Selections

Section 3.5 described the proposed generator module, which was represented by mathematical equations within a functional block diagram. The generator module is the analog circuit within the analog emulator that is mathematically equivalent to any given generator model. The advantage of this approach is that it allows the generator module to be built with fundamental building blocks, characterizing the components needed within the model, i.e. integrators, adders, multipliers, etc. These building blocks can easily be developed with analog circuits representing mathematical operations and functions.

This section details the selection of analog devices that are used in the proposed analog generator module and the analog circuits utilized with the analog emulator. All of the parts are readily available from different vendors. The selection of these devices occurred in 2005 and with the exception of the AD639 are still in production.

Table 5.1 describes the analog devices that are used in the analog circuits of the generator circuit building blocks. The devices listed are discussed in further detail in the following sections, followed by the development of the proposed analog generator module comprising of all the analog circuit building blocks.
Table 5.1: COTS CMOS Devices Used in Analog Generator Module

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Manufacturer</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM13700</td>
<td>National Semiconductor</td>
<td>Operational Transconductance Amplifier</td>
</tr>
<tr>
<td>AD639</td>
<td>Analog Devices</td>
<td>Universal Trigonometric Function Converter</td>
</tr>
<tr>
<td>AD734</td>
<td>Analog Devices</td>
<td>4-Quadrant Multiplier/Divider</td>
</tr>
<tr>
<td>LT1014</td>
<td>Linear Technologies</td>
<td>Precision Op Amp</td>
</tr>
<tr>
<td>MAX4603</td>
<td>Maxim Integrated Products</td>
<td>CMOS Analog Switches</td>
</tr>
<tr>
<td>LT1102</td>
<td>Linear Technologies</td>
<td>High Speed, Precision Instrumentation Amplifier</td>
</tr>
</tbody>
</table>

5.2.1. **Operational Transconductance Amplifier**

Instead of the typical operational amplifiers to realize some of the components needed, the operational transconductance amplifier (OTA) is used because of its ability to control its gain by an external current (or voltage). This extends the boundaries of the basic operational amplifier (op-amp) and makes realizable designs that were previously unobtainable. The OTA differs from the traditional op-amp, which is a voltage-controlled voltage source (VCVS). The OTA has the basic properties of a voltage-controlled current source (VCCS). While the op-amp behaves as a voltage source with a large gain (infinite for ideal), the OTA works as a current source with a finite transconductance gain, $g_m$, which is controllable via an external bias current, $I_{abc}$. Figure 18 shows a diagram of an ideal OTA’s circuit behavioral model (a) and its small-signal model (b), with both represented as a voltage-controlled current source.
The output current, $I_o$, is obtained by the product of the transconductance parameter, $g_m$, and the differential input voltage, $V_{in}$.

\[ I_o = g_m \cdot V_{in} \]  \hspace{1cm} (5.1)

The transconductance parameter can be increased or decreased as a function of the input voltage by varying the amplifier bias current, $I_{abc}$. The transconductance of the device can be considered as a gain and is dependent on a non-linear device constant, $\rho$ and the amplifier bias current [30].

\[ g_m = \rho \cdot I_{abc} \]  \hspace{1cm} (5.2)

Ideally, the desirable gain of an OTA, for a given $I_{abc}$, would always be constant, with a linear input-output relationship. Since this is not the case, measures need to be considered because of the errors that will result from the non-linear transconductance of the OTA. To increase the accuracy of the analog emulator and inherently the generator model, the transconductance gain needs to be defined. A detailed representation of the transconductance gain is derived by [31],

---

**Figure 18: Ideal OTA (a) Behavioral Model (b) Small-Signal Model**
$$g_m = \frac{I_{abn}}{2 \cdot V_T} \cdot \text{sech}^2 \left( \frac{V_{in}}{2 \cdot V_T} \right) \quad (5.3)$$

This equation illustrates that the gain is non-linear in nature and depends not only on the input voltage but also on the thermal voltage, $V_T$. The nature of the hyperbolic secant function limits the input range because the gain will rapidly decrease for small deviations of the input voltage as it diverges from zero.

The linear characteristics of the OTA greatly depend on how much error one is willing to accept. Many advances have been made in this regard. For example, the OTA selected in the thesis, National Semiconductor’s LM13700 [32], makes use of linearizing diodes that involve flattening the transconductance characteristic to achieve a wider input range and is capable of removing the temperature dependence. This occurs because the input transistors and the linearizing diodes have identical geometries that are subject to similar voltages and temperatures, but the limitations are that the signal current cannot exceed $\frac{1}{2}$ of the diode bias current, $I_D$, and the diodes must be biased with current. Below, Figure 19 describes the diode bias current

![Figure 19: LM13700 Differential Input Diode Linearization](image)
For the LM13700, the recommended linear approximation of the gain is 19.2. A comparison of the OTA gain factor, \( \rho \), (linear vs. non-linear) is illustrated in Figure 20.

\[
g_m = 19.2 \cdot I_{abc}
\]

(5.4)

![Figure 20: OTA Transconductance Gain Characteristics](image)

To ensure that the operation of the OTA is within a linear operating region, certain considerations need to be realized. The maximum device rating of the amplifier bias current for the LM13700 is 2mA. The amplifier bias current typically needs to operate in the range of 1\( \mu \)A to 1mA to minimize device offsets. In addition, with the gain of the OTA dependent on amplifier bias current, the output current of the OTA starts to saturate as it approaches the amplifier bias current. To avoid saturation the output current of the OTA cannot exceed the amplifier bias current. This circumstance can be observed in Figure 21.
The input-output characteristics of the LM13700 provide details concerning the input-voltage operating region to maintain a linear transconductance. In general, for a given maximum error, the linear differential input range of a differential input stage depends on the channel inversion of its transistors and at weak channel inversion [33]; the linear range is a few millivolts [34]. To minimize errors seen on the output current, the input voltage needs to be within ±25mV. This limitation imposed on the input voltage allows for ~5% maximum error on the output with linearizing diodes of the LM13700, as opposed to ~20% maximum error on the output without linearizing diodes in (5.3). As the
input voltage exceeds this condition, the error on the output current increases considerably. This linear operating region for two distinct amplifier bias currents is shown in Figure 22.

![Graph showing transfer characteristics for varying bias currents](image)

**Figure 22: LM13700 Transfer Characteristics for Varying Bias Currents**

With circuit design focusing on the preferred operating regions and linear behavior of the OTA, the internal device offsets present another issue that needs consideration. Any mismatch between the transistors on the differential input of the OTA will create an internal offset voltage. This voltage offset is transformed into current and amplified by the transconductance gain. A zero voltage input into the OTA results in a varying current offset seen on the output of the OTA directly affected by the amplifier bias current. One discrepancy between software simulation and hardware results, seen in
this thesis, is the offset characteristic of the LM13700. Figure 23 illustrates that the PSpice model of the LM13700 OTA behaves differently from what is observed in hardware. Figure 23 shows the offset current on the output modeled in PSpice increases with $I_{abc}$, while it decreases in hardware.

![Figure 23: LM13700 Offset Characteristics](image)

Many external designs, including trimmers, compensators, and feedback circuits, can be incorporated into the circuit to improve many of the disadvantages listed above. The approach of tuning circuits is typically valid for fixed gains, which negates device reconfigurability. One of the advantages of using the OTA for this application is the simple design. The basic building blocks of a rudimentary OTA consists of only nine transistors to create the differential input and four current mirrors as seen in Figure 24.
Figure 24: LM3080 Internal Building Blocks [35]

The simplistic design has allowed many improvements of the OTA design to expand its linear operating capabilities, remove the gain dependence on temperature, and eliminate internal offsets of the device. Multiple methods for improving the linear range have been proposed that can increase the linear input voltage to ±0.5V and even as high as ±8V [36], in some cases. One method to achieve increased linearity includes using the square-law MOS-input characteristic [37], where the differential input stage transistors are operating at strong inversion. Another common method includes the use of current mirrors [38] or programmable current mirrors [39-41], for which results have shown high linearity, high bandwidth, and wide-gain adjustment range varying multiple decades. Instead of modifying the structure of the OTA, sometimes feedback [36] and feed-
forward [42] techniques are utilized to force the OTA to follow linear characteristics. Lastly, a method for offset cancellation has been proposed in [43], which is capable of minimizing the offset for varying gains and not just one configuration. Results demonstrated that the amplifiers’ offset is eliminated and the transconductance is calibrated within two clock cycles.

The simplest way of solving these problems is the use of the improved OTAs with on-chip diode linearization, like the LM13700. This approach will be realized in this thesis for the verification of the analog emulator using commercially available parts. The disadvantages include narrow linear input voltages, offsets on output current, and temperature dependence of the gains. Note that the LM13700 is designed for high frequency applications and it contains extra circuitry, including protection circuits and buffers.

This thesis will take into account the deficiencies of the commercial OTA when analyzing the solutions of the power system emulation. The best technique for the final goal of a large-scale power system emulator would be the design of a custom OTA for VLSI implementation to focus only on the application of power system computation. Due to its versatility, the OTA is a very important building block of analog VLSI circuits and its primary use is for continuous-time linear and non-linear VLSI circuits with programmable characteristics [30].

5.2.2. Trigonometric Function

Another key building block for the analog emulator is the CMOS device capable of performing trigonometric functions. This is essential for the polar to Cartesian coordinate conversion. The device selected for this function is the Analog Devices
Analog Devices AD639 Universal Trigonometric Function Converter [44]. To achieve proper operation of the analog circuit, the AD639 is capable of performing the required sine and cosine trigonometric functions and has the additional capability of amplitude control through the application of an external voltage. This is an important aspect of the generator model as described in Figure 12.

Two AD639 chips will be used, one in a sine mode configuration with external amplitude control to calculate the real part of the complex generator voltage, and the second in a cosine mode configuration with external amplitude control for the calculation of the imaginary part of the complex generator voltage. The external amplitude control will dictate the internal generator voltage magnitude, $|E_c|$. The computer control voltage can be in the range of 10mV to 10V, for the desired amplitude scaling discussed in Section 4.4.1. This added feature in the AD639 allows for the reduction of devices needed within the generator model.

The angle input for the device is directly proportional to the input voltage. The input angle of a voltage uses a scaling factor of $50^\circ$/V, and the input voltage can be driven up to ±12V, or $600^\circ$. This device unfortunately does not have a commercial PSpice model available. One was created with ABM models and based on the device parameters from the datasheet. More information of this model can be found in Appendix A. An assessment of the hardware performance for typical input levels found that the device was capable of calculating the functions with errors $\leq 0.6\%$. The hardware results can be seen in Table 5.2.

Additional devices and circuits are summarized in the following sections with additional information in Appendix A.
Table 5.2: AD639 Hardware Results

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Calculated Outputs</th>
<th>Measured Outputs</th>
<th>% Error</th>
</tr>
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<tbody>
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<td>$</td>
<td>E</td>
<td>(V)$</td>
<td>$\delta$ (V)</td>
</tr>
<tr>
<td>2.005</td>
<td>0.000</td>
<td>0.00</td>
<td>2.005</td>
</tr>
<tr>
<td>2.005</td>
<td>0.052</td>
<td>2.60</td>
<td>2.003</td>
</tr>
<tr>
<td>2.005</td>
<td>0.104</td>
<td>5.20</td>
<td>1.997</td>
</tr>
<tr>
<td>2.005</td>
<td>0.155</td>
<td>7.75</td>
<td>1.987</td>
</tr>
<tr>
<td>2.005</td>
<td>0.206</td>
<td>10.30</td>
<td>1.973</td>
</tr>
<tr>
<td>2.005</td>
<td>0.296</td>
<td>14.80</td>
<td>1.938</td>
</tr>
<tr>
<td>2.005</td>
<td>0.398</td>
<td>19.90</td>
<td>1.885</td>
</tr>
</tbody>
</table>

5.2.3. Other Devices

With the two key components of the analog emulator selected, the remaining building blocks are basic functions requiring simple circuits. These circuits include:

- Analog multipliers to calculate the electrical power output of the generator.

- CMOS analog switches, which will be used for two functions: generator on/off state, and generator fault conditions.

- Operational amplifiers will be used in multiple circuits including: summing (addition) amplifiers, difference (subtraction) amplifiers, and buffers.

- High speed, precision instrumentation amplifiers will be used for current measurements on the output of the generator terminals.

The devices selected for these analog building blocks are outlined in Table 5.1. The configuration of each device are fundamental circuits that can be found in Appendix A and require little explanation. A main concern when designing these circuits within the
generator module is the impedance matching between each block. This aspect is important for maximizing the transfer of power from the source to the load. If impedance matching is neglected, then problems could arise such as constant sources becoming loaded or signal attenuation and noise appearing in the circuit.

Having the appropriate devices selected, two circuits for the analog generator module will be discussed, followed in later chapters with steady-state emulation results and recommendations for future development.

5.3. Generator Module

With the generator model developed, scaling parameters defined, and device components selected, two different generator circuits will be discussed. The first circuit is an example of a simple single-machine to infinite bus. The purpose of this circuit is to verify the proper operation and calculation of the generator’s electrical angle. The second circuit is the proposed generator module that will be used for multi-machine power system emulation.

5.3.1. Generator to Infinite Bus

The generator to infinite bus model is a simple circuit based on the functional block diagram from Figure 11. This example is helpful in many ways because it can be tested within a single circuit, not requiring additional power system analog circuits (i.e. transmission lines or loads) and it incorporates power system scaling and generator parameters. This example model is used not only to verify the solution of the swing equation (3.3), but also proves and validates the scaling parameters described in Section 4.4.
This circuit will mimic the behavior of a generator delivering power to an infinite bus through a transmission line. In this case, the generator’s MVA rating is relatively small so it can be expected not to significantly affect the voltage and frequency of the larger system. This assumption allows the bus voltage to be independent to how the generator is adjusted, effectively making the infinite bus an ideal voltage source. The one line diagram of this example can be seen in Figure 25.

![One line diagram of a generator to infinite bus system](image)

**Figure 25: Generator to Infinite Bus Line Diagram**

For this single-machine power system, the calculation of the steady-state solution of the electrical angle of the generator can be found by solving the instantaneous generator power for the system. This occurs when there is a balance between the mechanical power input and the electrical power output. For a given mechanical input power, the steady-state solution of the electrical angle can be found with known system parameters.

\[
\begin{align*}
    P_m & = \frac{|E||V|}{(X'_d + X_L)} \sin \delta^o \\
    P_m &= P_{e,max} \sin \delta^o \\
    \Rightarrow P_{e,max} &= \frac{|E||V|}{(X'_d + X_L)}
\end{align*}
\]

(5.6)
The analog circuit for the single-machine power system will consist of four OTAs, a trigonometric converter, resistors, and capacitors, as seen in Figure 26. The selection of CMOS device parameters depend on multiple factors. For instance, the selection of $R$ is used to scale the input of the double integer from a current to a voltage, as well as scale the input of $OTA_{m1}$ within its linear operating region. The resistors $R_1$ and $R_2$, are used as a voltage divider to scale the input of the $OTA_{mA}$. The selection of $C_1$ and $C_2$, changes the integration time of the circuit, which directly influences the time scaling or computational speed up of the generator model.

The equation describing the behavior of the circuit, includes the output of the double integration process, $V$, representing the electrical angle and is calculated in the following manner that is analogous to (4.15).
\[
\delta \equiv V = \frac{g_{m1} \cdot g_{m2}}{C_1 \cdot C_2} \int \int (I_m - I_e(V)) \, dt \, dt 
\] (5.7)

To attain the difference between the mechanical input power and the electric output power of the generator within the circuit, real power is quantified as a current. This introduces a circuit scaling parameter, \( K_p \), a constant ratio between the maximum circuit current, \( I_{\text{max}} \), and the maximum real world power, \( P_{\text{max}} \), already normalized to per-unit quantity. The use of \( K_p \) allows for the limiting of the current level within the circuit as well as dictates the maximum real world power quantity that can be emulated within the circuit. This incorporates the magnitude scaling and parameter scaling of power to current as described in Section 4.4.

\[
K_p = \frac{I_{\text{max}}}{P_{\text{max}}} 
\] (5.8)

Next, the controllable gains need to be described, which define the power system parameters within the analog generator circuit. The gain representing the maximum electrical power output for a single-machine power system (5.6), \( P_{\text{e,\,max}} \), is transformed into the maximum current gain parameter \( A \), which is equivalent to \( I_{\text{e,\,max}} \) for a set of specific power system parameters via \( K_p \). With this approach, the maximum allowable current, \( I_{\text{e,\,max}} \), will be controlled through the gain of the OTA, \( g_{mA} \). This can be changed for different power system parameters in the following manner using equations (5.6) and (5.8).
\[ A = K_p \cdot P_{e,\text{max}}; \quad g_{m_A} = A \cdot \frac{R_1 + R_2}{R_2} \]

\[ g_{m_A} = \frac{K_p |E|V |(R_1 + R_2)}{(X_d + X_L)R_2} \]

(5.9)

In this thesis, the two gains, \( OTA_{m1} \) and \( OTA_{m2} \), within the double integrator will always be considered identical to one another for simplicity. These gains could eventually be decoupled from one another assigning time scaling and generator parameters separately to different gains. Using equations (4.15), (5.7), and (5.8), the gains of OTAs in the double integrator can be characterized with the following equation.

\[ M = \frac{H}{\pi f_o}; \]

(5.10)

\[ g_{m_1} = g_{m_2} = \sqrt{\frac{C_1 \cdot C_2 \cdot \tau^2 \cdot V}{K_p \cdot M \cdot R \cdot \pi}} \]

For this simple power system, the real world power system parameters are directly associated with a controllable gain parameter and the generator inertia constant, \( M \), and the scaling parameters connected with another controllable gain parameter. This representation allows for a completely reconfigurable classical generator model that can easily be configured and can provide faster than real-time power system transient stability results. The following section defines a generator module circuit that can be used for large-scale power systems using other reconfigurable circuits, such as transmission lines and loads.
5.3.2. Generator Module for Multi-Machine Power Systems

The generator module will consist of the circuit representation of the proposed generator model in Figure 12. This circuit module is much larger and more detailed than the generator to infinite bus system. This module includes circuitry for calculation of the swing equation, real and reactive power calculation, output current measurements, and switching controls. The generator module can be used in a wide variety of power system configurations and conditions, but mainly this thesis will focus on a common 3-bus power system example including 1 reference generator (Slack Bus), 1 generator module (PV Bus), 3 transmission lines, and one load as seen below.

![IEEE 3-Bus Power System Emulator Line Diagram](image)

The double integration of the difference between the mechanical and electrical power does not change from the previously described circuit. The calculation of the two integrator gains, $g_{m1}$ and $g_{m2}$, is the same as in equation (5.10), but the scaling factor, $K_p$,
is defined differently. Beforehand, the transformation of current to power defined $K_p$, which included the normalized magnitude scaling of the power system. In this circuit, the $P \rightarrow I$ transformation now factors in the physical to normalized magnitude scaling, as well as per-unit to appropriate circuit magnitude scaling.

$$I_{\mu A} = \frac{P_{MW} \cdot K_p}{S_b}; \text{ where, } K_p = \frac{V_k^2}{Z_k}$$

(5.11)

$$I_{\mu A} = P_{p.u.} \cdot K_p; \text{ where, } P_{p.u.} = \frac{P_{MW}}{S_b}$$

In (5.11), $V_k (V/p.u.)$ and $Z_k (k\Omega/p.u.)$ were described in section 4.4.1, which allow $K_p$ to relate the circuit current ($\mu A$) to represent a per-unit quantity (p.u.). With a base power selected, $S_b$, and a given real world power, $P_{MW}$, the result is a per-unit power quantity, $P_{p.u.}$. The product of the per-unit power value and the $P \rightarrow I$ transformation parameter results in the current level within the circuit representing a real world power quantity. This association is an essential feature to the analog emulator that allows for flexibility in associating the constraints of the physical power system to the limits of the analog emulator circuit.

Next is the overview of the required interface and feedback that is used to connect the generator to the power system network using DC emulation as described in Section 4.2. The output of the generator supplies real and imaginary voltage to the bus terminal. The real voltage of the generator is supplied to two of the four DC networks, representing the real and imaginary network impedances, and the imaginary voltage is supplied to the other two DC networks, also representing the real and imaginary network impedances.
This described topology can be distinguished in the following figure. The four DC networks are needed for the equivalent of a lossy power system network, while only two networks, specifically DC Network 2 and 3 are required to emulate a lossless power system network.

Figure 28: Three Bus DC Emulation Topology

With this network topology, to obtain the result of the supplied electrical power output of the generator requires placing current sensors on the four output terminals of the generator along with the result of equation (4.3). Overall, the measured output currents, voltages, and the calculated electrical power (represented as a current) has a
unity feedback in the circuit. Note that each circuit component has different gains as shown in Table 5.3 and Figure 29.

Table 5.3: Electrical Power Output Calculation Circuit Gains

<table>
<thead>
<tr>
<th>Circuit Gain Parameter</th>
<th>Gain Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measurement Resistor</td>
<td>100</td>
</tr>
<tr>
<td>Instrumentation Amplifier</td>
<td>10</td>
</tr>
<tr>
<td>Current Calculation</td>
<td>10</td>
</tr>
<tr>
<td>Multiplier</td>
<td>0.1</td>
</tr>
<tr>
<td>Resistor Divider</td>
<td>0.1</td>
</tr>
<tr>
<td>OTA</td>
<td>0.01</td>
</tr>
<tr>
<td>Overall Feedback</td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 29: Electrical Power Output Feedback Circuit
The first circuit provides the current measurement of the output power at the generator terminals. This circuit uses an instrumentation amplifier, shown in Figure 50 in Appendix A. The output of this circuit is a voltage representing the current flow for each of the DC networks. These four DC network currents need to be combined into the real current and imaginary current providing the complex power of the generator. The calculation of the real and imaginary parts of the complex current is derived from equations (4.3) and reciprocal of (4.6).

\[
\begin{align*}
I &= Y \cdot V \\
(I_{re} + jI_{im}) &= (Y_{re} + jY_{im}) \cdot (V_{re} + jV_{im}) \\
&= (V_{re}Y_{re} - V_{im}Y_{im}) + j(V_{re}Y_{im} + V_{im}Y_{re}) \\
&= V_{re}Y_{re} \{ \text{Network 1} \} I_{re} + jV_{re}Y_{im} \{ \text{Network 3} \} I_{im} + jV_{im}Y_{re} \{ \text{Network 4} \} I_{im} + jV_{im}Y_{im} \{ \text{Network 2} \} I_{im}
\end{align*}
\]

\[
R_{re[ij]} = \frac{1}{\text{Re}(Y_{ij})} = \frac{R_{ij}^2 + X_{lij}^2}{R_{ij}} \\
R_{im[ij]} = \frac{1}{\text{Im}(Y_{ij})} = \frac{R_{ij}^2 - X_{lij}^2}{X_{lij}}
\]

The term, \(Im(Y_{ij})\), in (4.6) produces a negative current in the DC networks 2 and 3, which yields the following characterization.

\[
\begin{align*}
I_{re} &= I_1 + I_2 \\
I_{im} &= I_4 - I_3
\end{align*}
\]
Op-amps are used in adder and difference amplifier configurations, with circuit diagrams located in Appendix A, for the calculation of the real and imaginary currents. The electrical power output of the generator is computed using equation (3.4), and utilizes two multipliers that are capable summing another signal with the output as shown in Appendix A.

\[
Re\{S\} = Re\{V \cdot I^*\} \\
P_e = E_{\text{Real}} \cdot I_{\text{Real}} + E_{\text{Imag}} \cdot I_{\text{Imag}} \\
P_e = |E_G| \cdot \cos \delta \cdot Re\{I\} + |E_G| \cdot \sin \delta \cdot Im\{I\}
\] (3.4)

Before the electrical power, represented as a voltage is transformed into a current, a resistor divider is required for two purposes; scale the voltage within the linear input operating range of the OTA and provide necessary gain for the overall feedback.

With all of the gain components defined for each circuit, the OTA requires a fixed gain of 0.01 mhos. Using equation (5.4), the resulting amplifier bias current that needs to be supplied is 520.83 μA. This gain is within the operational limits of the OTA and can easily provide up to ±500 μA for the electrical power represented as a current in the circuit. This corresponds to a threshold for the output power of the generator module circuit of approximately -500 μW to +500 μW because of overall feedback gain of the electrical power output calculation equals one as described in Table 5.3. This corresponds to a 1 to 1 relationship between the actual analog circuit power output (μW) and the electrical current (μA) representing the electrical output power of the generator. Since the output voltage (real and imaginary) is dependent upon the scaling of $|E_G|$ (constrained by
the computer control voltage of -10V to -50mV and 50mV to 10V), the output current of the module is dictated by the following equation.

\[ P_{out} = \text{Re}\{V_{out}\} \cdot \text{Re}\{I_{out}\} + \text{Im}\{V_{out}\} \cdot \text{Im}\{I_{out}\} \]  \hspace{1cm} (5.13)

With both generator module circuits designed, appropriate devices selected, and reconfigurable parameters defined, the verification and validation of both designs are desirable. Additional information regarding the switching conditions of the generator and the initial conditions of the terminal voltage magnitude and phase can be found in Appendix B. The next chapter will include steady-state emulation results for both designs, along with known limitations, which will be followed by the conclusion and recommendations for future development.
6. VALIDATION OF ANALOG GENERATOR MODELS

6.1. Overview

This chapter presents the verification and validation of the analog generator model presented in this thesis to be used in analog power flow computation. Software and hardware tests results are provided and compared to ideal and calculated results. The software tests were performed using PSpice with appropriate device models and the hardware tests were performed with an OTA based analog generator model. These tests incorporate the previously described scaling methods to operate within the limitation of the analog hardware. If scaling is not applied appropriately, the devices would saturate or become damaged which would invalidate the results of the load flow computation. In particular, tests results are provided for the single-machine to infinite bus and multi-machine power system examples.

This chapter is divided into two sections. The first section focuses on the single-machine to infinite bus example. This circuit is a self-contained feedback loop that emulates the parameters of the generator model. One example is provided to verify the feasibility of the analog devices and scaling issues used within the generator model. The second section includes the generator module that connects to the analog power system network. More detailed examples and model behaviors will be identified within this section.

6.2. Generator to Infinite Bus Testing

The proposed method for a reconfigurable classical generator model has been tested in a single-machine power system. These are only preliminary results, which will
later include a multi-machine power system example. The purpose of this example is to exhibit the viability of this approach through characterization of its fundamental behavior, which will be recognizable in larger scaled systems. The circuit and equations under test are described in Section 5.3.1. The generator to infinite bus results will be compared to results from a simple power system example [21]. This example uses the power system parameters listed in Table 6.1.

<table>
<thead>
<tr>
<th>Power System</th>
<th>Circuit Emulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>E_G</td>
</tr>
<tr>
<td>$</td>
<td>V</td>
</tr>
<tr>
<td>$X_d \ (\text{p.u.})$</td>
<td>$g_{m1} \ (\text{mho})$</td>
</tr>
<tr>
<td>$X_L \ (\text{p.u.})$</td>
<td>$g_{m2} \ (\text{mho})$</td>
</tr>
<tr>
<td>$H \ (\text{sec})$</td>
<td>$K_p$</td>
</tr>
<tr>
<td>$P_m \ (\text{p.u.})$</td>
<td>$v \ (\text{V})$</td>
</tr>
<tr>
<td>$f_0 \ (\text{Hz})$</td>
<td>$\tau$</td>
</tr>
<tr>
<td>$A \ (\mu A)$</td>
<td>$I_m \ (\mu A)$</td>
</tr>
<tr>
<td>$g_{mA} \ (\text{mho})$</td>
<td>0.0130</td>
</tr>
</tbody>
</table>

Listed above, are both the real world power system parameters and the associated scaled circuit parameters. The circuit parameters where selected to ensure the devices are within their respective linear operating regions. The circuit proposed in Figure 26 was designed in software and the circuit emulator was simulated. This circuit was also built in hardware and tested. The results of the software simulation within PSpice will be compared to results obtained using PSpice Analog Behavior Models (ABM) and equation
This comparison is validated from previous work [5] conducted using Analog Behavior Models of sample power systems, where the results obtained compared rather favorably with traditional load flow solvers such as PSS/E and PowerWorld.

For this example, the mechanical input power is fixed constant at 0.5 p.u. while the emulator solves for a steady-state solution. Figure 30 shows the transient response of the generator settling to the steady-state solution of (a) the real world power system and (b) the analog emulator. With both converging to approximately the same steady-state solution, it is clearly shown that the analog emulator is capable of solving the electrical angle of the swing equation 5000 times faster than the actual power system for the selected \( \tau \) in this example. This demonstrates the capability of the computational speedup the analog emulator possesses with respect to real-time.

![Figure 30: Single-Machine Steady-State Solution (a) Actual (b) Scaled](image-url)
Upon further examining of Figure 30, it can be seen that the steady-state results does not look to match up accurately. This is also true for the hardware results that can be seen in Figure 31. The top signal (1) of the scope capture is the actual hardware measurement of the electrical angle. The bottom signal (M) is the math reference signal that represents the electrical angle as a 1:1 ratio of volts to degrees.

The disparity between the different methods can simply attributed to the offset present within the OTA and the difference between the actual hardware device and PSpice model, as explained in Section 5.2.1 and Figure 23. With the results tabulated in Table 6.2, the outcome is similar to the expected results taken the offset into consideration. The PSpice model has a positive offset for a given amplifier bias current, which the example has a positive offset from the desired solution. In addition, the
hardware has a negative offset for a given OTA bias current, which the electrical angle measured in hardware was lower than the desired solution.

Table 6.2: Single-Machine Example Results

<table>
<thead>
<tr>
<th>Method</th>
<th>Delta (deg)</th>
<th>Offset (deg)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Calculation</td>
<td>22.885</td>
<td>-</td>
</tr>
<tr>
<td>PSpice ABM</td>
<td>22.886</td>
<td>0.0</td>
</tr>
<tr>
<td>PSpice Circuit</td>
<td>27.787</td>
<td>+4.0</td>
</tr>
<tr>
<td>Hardware Circuit</td>
<td>16.000</td>
<td>-6.8</td>
</tr>
</tbody>
</table>

This example is provided to demonstrate the feasibility of using OTAs and other analog CMOS devices in such a configuration to emulate power system components. The results conclude that the accuracy of the solution can be increased by quantifying the offsets present in the model. This is one recommendation for future work. With the concept of an analog emulator capable of providing valid power system stead-state solutions, further analysis will continue on the generator module. The next section presents and discusses the results of the generator module that will be used in large-scale power systems.

6.3. Generator Module Circuit Validation Testing

This section presents the results from the tests performed on the generator module. Two different configurations will be tested, lossless and lossy generator models, and compared to PSpice. The test performed on the generator module will include parametric sweeps on each of the individual control inputs to the generator circuitry ($P_m$, $E_g$, $I_{abc}$) and measurements on all of the output monitors of the generator circuitry ($P_e$, $E_{abc}$).
for a selected fixed load impedance on the generator’s network terminals. This will quantify the input/output voltage characteristics of the generator module without any reference or scaling to power system parameters. Figure 32 describes the connection setup for testing of the generator module. Using National Instruments PXI PC running LabVIEW, control and monitoring of the generator parameters can easily be achieved using National Instruments Analog Input (AI) and Analog Output (AO) Data Acquisition Cards (DAQ).

![Diagram showing the connection setup for testing of the generator module.](image)

Using the PXI portion of the chassis for computer control and data acquisition, the SCXI slots supply power and signal interface to the custom SCXI Generator Module PCB. A picture of the actual Generator Module PCB is shown in Figure 33 with the lossless/lossy configuration jumpers labeled.
### 6.3.1. Lossless Configuration

The lossless configuration of the generator module circuitry utilizes only the DC Networks 2 and 3 as described in Section 5.3.2. This is accomplished by changing board jumper settings that will remove (or ground) the lossy network currents (from the real part of the complex network admittance), $I_I$ and $I_4$, as redefining equation (5.12) as the following.

$$
I_{re} = 0 + I_2 \rightarrow I_{re} = I_2, \\
I_{im} = 0 - I_3 \rightarrow I_{im} = -I_3
$$

(6.1)
For the lossless test setup, the following conditions were used. Each generator control input parameter was set to a selected fixed voltage. In addition, selected fixed load impedances are connected to Network 2 and 3, with Network 1 and 4 connected to ground. The load resistances used for this test were $R_2 = 17.7\,\text{k}\Omega$ and $R_3 = 64.7\,\text{k}\Omega$.

Figure 34: Lossless Generator Module Configuration
The first test performed kept the generator voltage magnitude, $E_G$, and amplifier bias current, $I_{abc}$, both constant while varying the generator mechanical input power, $P_m$. Figure 35 illustrates the ranges of the mechanical input power has a range of ±1V before the electrical power angle reaches emulation device saturation. Both hardware and PSpice simulation results behave similarly concerning the input/output characterization of the generator module circuitry. Note that to guarantee convergence for a wide range of generator power, the use of initial conditions on the generator electrical angle solution is required to avoid the limitations on the emulation circuitry. The use of initial conditions is briefly discussed in Appendix B.

![Graph](image)

Figure 35: Hardware and PSpice Power Angle vs. Mechanical Input Power
Figure 36 depicts the electrical output power as a function of the mechanical input power, both emulated by circuit voltages. Within the range of ±1V, before device saturation, the electrical output power results of the Hardware and PSpice track each other with some offset to the OTA devices. The difference of solutions after device saturation between the Hardware and PSpice results can be attributed to various issues. The hardware is susceptible to noise, parasitics, device sensitivity, etc, while the PSpice simulations assume ideal signal measurement and circuit operating conditions. Especially when operating at low voltages, PSpice may reach an ideal operating solution while the Hardware results will be affected by measurement noise, device saturation, and other parasitics, which were not modeled within the software.
Figure 37 characterizes the reactive output power over the range of the mechanical input power. Again, the PSpice model and hardware circuitry behave similar to one another within the range of ±1V of the mechanical input power.

Figure 37: Hardware and PSpice Reactive Power vs. Mechanical Input Power
Figure 38 illustrates the generator power angle, $\delta$, over the range of the amplifier bias current, $I_{abc}$. Again, the PSpice model and hardware circuitry behave similar with both behaving in a linear fashion with a slight drift due to the offset current across the range of the amplifier bias current.

![Figure 38: Hardware and PSpice Power Angle vs. Amplifier Bias Current](image-url)
Figure 39 plots the Generator Power Angle, $\delta$, against the Internal Generator Voltage Magnitude, $|E_G|$. This outcome is expected because as the $|E_G|$ decreases $\delta$ will increases, eventually saturating the circuit output. Larger generator angles can be achieved with the use of initial conditions as described earlier. The PSpice model slightly differs from the hardware circuitry due to the different op-amp $V_{cc}$ voltages, +15V for PSpice vs +10V for hardware and the PSpice Internal Generator Magnitude is $E_G$ without the absolute value calculation, resulting in the different behavior for the negative voltages of $|E_G|$.

![Figure 39: Hardware and PSpice Power Angle vs. Internal Voltage Magnitude](image-url)
Figure 40 shows the plot of the Electrical Power, $P_e$, versus the Internal Generator Voltage Magnitude, $|E_G|$. The result observed is expected because as the $|E_G|$ decreases $\delta$ increases, eventually saturating the circuit’s amplifier output. Larger generator angles can be achieved with the use of initial conditions as described earlier. The PSpice model slightly differs from the hardware circuitry due to the different op-amp $V_{cc}$ voltages, +15V for PSpice versus +10V for hardware and the PSpice Internal Generator Magnitude is $E_G$ without the absolute value calculation, resulting in symmetric behavior instead of saturation for negative voltages of $|E_G|$.

Figure 40: Hardware and PSpice Electrical Power vs. Internal Voltage Magnitude
Figure 41 plots the Reactive Power, $Q_e$, versus the Internal Generator Voltage Magnitude, $|E_G|$. The hardware results are expected because as $|E_G|$ decreases, $\delta$ will increase, again saturating the circuit’s amplifier output. This explicitly shows the limitations of the analog circuitry saturation points requiring the use of initial conditions.

![Graph of Reactive Power vs. Internal Voltage Magnitude](image)

**Figure 41: Hardware and PSpice Reactive Power vs. Internal Voltage Magnitude**

In summary, the tests conducted on the generator module in hardware exhibited similar input and output characteristics to the PSpice simulations and were used for comparison and verification of the circuit characteristic and performance, which will be used to emulate scaled power system parameters. The control of the mechanical input power, $P_m$, exhibits an operating region slightly better than $\pm 1V$ before the output measurement saturated for both PSpice analysis and hardware testing. The control of the internal generator voltage magnitude, $|E_G|$, demonstrates that for magnitudes less than 1.7V, the amplifier’s output will be saturated. The control of the Amplifier Bias Current
across the wide operating range of ±10V showed very little deviation of the measurement, but this is expected, as the OTA’s output offset current is a function of the bias current.

6.3.2. Lossy Configuration

PSpice and Hardware validation for the lossy configuration is similar to the lossless configuration and the results are presented in Appendix C. The most important difference between the two tests is the addition of fixed load resistors ($R_i$ and $R_d$) on the output Networks 1 and 4. Performance results are almost identical to the lossless configuration results.

6.4. Generator Module with Network and Load Testing

The preceding tests focused on testing the generator model separately and determining the input/output characteristics of the generator module. This section now introduces additional transmission line and load modules to create a simple 3-bus power system analog emulation. The tests were conducted using the generator module, a network module (transmission lines) [45], and an OTA-based constant current load module [46]. The slack bus is represented by DC voltage sources.

The configuration of the generator, network, and load modules included all setting according to the PowerWorld system parameters in Table 6.3 and the analog emulation scaling factors in Table 6.4. The lossless configuration was used for transmission line models for simplification and the 3-Bus PowerWorld one-line diagram is shown in Figure 42.
Table 6.3: PowerWorld 3-Bus Parameters

<table>
<thead>
<tr>
<th>Buses</th>
<th>Real</th>
<th>Imaginary</th>
<th>1.0 V p.u.</th>
<th>10 Degrees</th>
<th>130 MW</th>
<th>400 MVAR</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) Slack</td>
<td>1.00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(2) Generator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(3) Load Constant Current</td>
<td>100 MW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Lines

<table>
<thead>
<tr>
<th>Lines</th>
<th>Real</th>
<th>Imaginary</th>
<th>Ω p.u.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line 1-2</td>
<td>0.00</td>
<td>0.22</td>
<td></td>
</tr>
<tr>
<td>Line 1-3</td>
<td>0.00</td>
<td>0.15</td>
<td></td>
</tr>
<tr>
<td>Line 2-3</td>
<td>0.00</td>
<td>0.19</td>
<td></td>
</tr>
</tbody>
</table>

Figure 42: PowerWorld 3-Bus Simulation
Using LabVIEW software, a custom graphical user interface (GUI) has been created to interface with the data acquisition and control of the analog emulation with the hardware modules as shown in Figure 43. The software was designed to have all inputs represented in the similar configuration parameters of PowerWorld such as generator/load power and transmission line reactance using the equations provided in this research. This provides the correct translation of the parameters using the scaling factors previously discussed to the proper analog voltages and currents.
The main panel of the interface was specifically designed for the 3-bus power system emulator consisting of three transmission lines, two generators (one slack) and a single load that have reconfigurable parameters. The controls of the emulator are located on the bottom of the panel allowing the user to select lossy or lossless configuration, start integration (find solution), create faults, set initial conditions, and trigger an external scope. The configurable parameters of the generator consist of real power output (MW), voltage magnitude (p.u.), system frequency (Hz), generator moment of inertia (sec), and starting angle (deg.). Similarly, the transmission lines resistance (p.u.) and reactance (p.u.), the slack bus voltage magnitude (p.u.) and angle (deg.), and the load’s real power (MW) and reactive power (MVAR) are user configurable parameters. The panel also displays the solutions of the generator’s real power output (MW), reactive power output (MVAR), and electrical angle (deg.) for the given system parameters when the emulator is running.

Other panels within the GUI include the entering of scaling parameters, selecting of fault initiation and duration timing parameters, and external scope screenshot. The following table includes all of the selected scaling parameters for this 3-bus example.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_b$</td>
<td>100</td>
<td>MVA</td>
</tr>
<tr>
<td>$V_b$</td>
<td>138</td>
<td>kV</td>
</tr>
<tr>
<td>$V_k$</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>$Z_k$</td>
<td>16000</td>
<td>kOhm</td>
</tr>
<tr>
<td>$\nu$</td>
<td>3.6</td>
<td>Volt/Deg</td>
</tr>
<tr>
<td>$\tau$</td>
<td>1000</td>
<td></td>
</tr>
</tbody>
</table>
With the proper generator voltages applied to the emulator circuitry, the generator and load bus voltages were measured and compared with the steady-state results from PowerWorld in Table 6.5. From this example, the results of the emulator compare favorably to those achieved by using PowerWorld. Based on multiple emulator runs, the results are repeatable and consistent for various cases. The bus voltages are typically within a few percent and the angles are within a couple of degrees of the results obtained from a digital power flow solver.

### Table 6.5: PowerWorld and Hardware Emulator 3-Bus Result Comparison

<table>
<thead>
<tr>
<th></th>
<th>PowerWorld</th>
<th>Emulator HW</th>
<th>Difference</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Generator</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Real Voltage (p.u.)</td>
<td>0.946</td>
<td>0.937</td>
<td>0.008</td>
<td>0.85</td>
</tr>
<tr>
<td>Imaginary Voltage (p.u.)</td>
<td>0.325</td>
<td>0.349</td>
<td>0.020</td>
<td>5.73</td>
</tr>
<tr>
<td>Angle (degrees)</td>
<td>18.97</td>
<td>20.40</td>
<td>1.230</td>
<td>6.03</td>
</tr>
<tr>
<td><strong>Load</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Real Voltage (p.u.)</td>
<td>0.650</td>
<td>0.655</td>
<td>0.005</td>
<td>0.76</td>
</tr>
<tr>
<td>Imaginary Voltage (p.u)</td>
<td>0.104</td>
<td>0.102</td>
<td>0.003</td>
<td>2.94</td>
</tr>
</tbody>
</table>

The emulation results are very close to the PowerWorld results and component tolerances and OTA nonlinearities are introducing most of the discrepancies seen here. Further refinement of the hardware including more accurate analog devices and measurement sensing would significantly improve these results.

Each of the test results presented in this chapter verify the functionality and reconfigurability of the generator model independently and as an integrated power system as presented in this thesis. All of the hardware emulation results, while including some error, are relatively close to the expected digital power flow results. With further
development, the computational accuracy of these circuits could be improved and implemented within a single VLSI chip to yield even better results of larger power systems.

Stage II realizes the verified analog behavior models and develops analog circuitry to replace the building blocks assembled in the previous stage. Using CMOS devices and software packages, the design, simulation, and PCB layout of power system components, i.e. generators, loads, transmission lines, etc, can be achieved. This development stage is broken up into two parts entailing circuit modeling and simulation and PC board development and emulation, which is the primary focus of this thesis.
7. CONCLUSIONS AND FUTURE WORK

7.1. Conclusions

This thesis explored the implementation of modeling generators for solving large-scale power systems in analog emulation. An overview of classical generator models provided insight into the methodology of analog model behavior and the concept of reconfigurable generator models. The application of OTAs enhances the flexibility within the generator model. Applying the reconfigurable model to a previously proposed analog emulation of power systems provided a scaled reconfigurable generator model in analog circuitry.

Software and hardware development of a reconfigurable analog generator model using OTAs was verified along each development stage. Simulation and hardware results validated the design along with the implementation of small power system example. A complete PCB generator module was constructed using off-the-shelf electronic components and tested with other power-system network prototype modules. The provided results compared favorably with traditional power system commercial software.

The simulation and hardware results also demonstrated the advantages and limitations of current commercial devices. Tradeoffs were made between accuracy and computational speedup. Limitations shown included the limited linear operating range of the OTA, offsets due to non-linear transconductance, and the application design of commercial OTAs. The commercially available CMOS OTAs are designed for high frequency applications that include control and protection circuits not necessary for power system analog emulation. This introduces the offsets and limited linear operating conditions that were experienced within the design of the generator model. Development
of a basic OTA will simplify the circuit design of the OTA, reduce errors from unnecessary features, and allow for the additions of improvements just described.

All the described limitations and improvements are relatively simple for CMOS components and there properties are advantageous for implementation with VLSI technology. This follows along the PSoC development process with the next development stage involving the transfer of the circuit realization into a VLSI design. Using this VLSI technology, all the generator building blocks (OTAs, resistors, and other CMOS devices) can be implemented with a single VLSI chip to contain many various generator models that can be configured, controlled, and monitored during analog emulation of power system networks.

7.2. Summary of Research Contributions

This work is an extension of research previously developed in the field of analog computation for power systems. Furthermore, the work presented is part of a larger project designed to develop CMOS analog models representing various power system components, which will be connected into power system networks. Highlighted below are some key contributions that have been made in this field of research.

- Developed a low cost, reconfigurable analog hardware representation of a classical generator model.
- Incorporated the capability of PV (regulated) and PQ (non-regulated) generator modes.
- Validation and verification of PV generator model analog emulation technique suitable for VLSI implementation.
7.3. Future Work

This research could continue in a few different directions. The next reasonable step for this research would be a VLSI implementation of the generator model for the purpose of a large power system network with transmission lines and loads on a single analog design. This would require designing a custom VLSI chip and its fabrication. In addition, the realization of efficient control and data acquisition schemes would need to be developed to maximize the speed of the analog solution. Furthermore, improvements to the reduction of device offsets would improve the precision of the analog emulator.

Another branch of work would investigate the transient analysis and stability of the generator model, instead of the steady-state analysis as seen in Appendix B. Preliminary research can examine the critical clearing time required for transient stability of first swing dynamic responses of analog components and later include analysis of multi-machine dynamics of larger power systems.

In this thesis, the presented second-order generator model only included the internal impedance and simplified swing dynamics of the generator. Further research could incorporate other real world generator characteristics including damping, an exciter, and a governor. Additionally, complex feedback and control algorithms could be included within higher-order generator models.
LIST OF REFERENCES


Conference on Electronics, Circuits and Systems, University of Patras, Greece, pp. 1321-1324, September 1999.


This section illustrates the various circuit models designed within PSpice. The simulation results of the generator model use the following circuits as described in Chapter 5. The circuits are reasonably simple and self-explanatory. Note that the Amplitude Preset $|E_G|$ does not include the absolute value as implemented in the hardware circuitry.

![Figure 44: ABM AD639 Cosine PSpice Model](image)

![Figure 45: ABM AD639 Sine PSpice Model](image)
Figure 46: LT1014 Difference Amplifier PSpice Circuit

Figure 47: LT1014 Summing Amplifier with Inverting Buffer Output PSpice Circuit
Figure 48: LM13700 Integrator PSpice Circuit

Figure 49: ABM AD734 Multiplier PSpice Model
Figure 50: LT1102 Instrumentation Amplifier Current Measurement PSpice Circuit
APPENDIX B: GENERATOR INITIAL CONDITIONS AND SWITCHING

The use of analog switches within the generator module introduces additional beneficial features. First, the use of a switch to create a fault at the generator allows for steady-state fault analysis and provides the capability of future studies to investigate transient stability analysis of the generator. Second, the use of switches on the integrating capacitors allows for the control of the initial voltage on the capacitors. With this feature, if the power system solutions are far enough apart to cause saturation, the generators are capable of starting at an initial condition that is close to the power system operating points.

An example of this issue, in hardware, can be seen by the limitations of the power angle’s voltage saturation for varying conditions in Figure 35 and Figure 39. With device saturation as a limitation and the scaling parameters selected, the power angle in degrees is limited approximately 50º, including the first swing peak deviation. For a steady-state solution greater than 25º with a first swing delta over 20º would reach device saturation and the generator conditions would run away. Using switches with voltage inputs on the integration capacitors, an initial condition can be applied on the emulator to solve the final solution without convergence/saturation issues. Figure 51 shows that an initial condition of 10º was applied to the circuit before the power flow emulation was initiated. This allows the analog emulation to reach a higher solution beyond the device saturation limits for a given configuration.
The generator model designed and proposed in this thesis also has the capability of performing fault analysis. An example of this can be seen in the figures to follow. Initial PSpice simulations were performed introducing different fault duration into the power system simulation. Figure 52 shows two power system conditions, one with a fault duration of 240μs (emulation duration, not real world) and another fault duration of 245μs.
This simulation demonstrates the model's ability to perform transient stability and fault analysis. With the fault duration of 240μs, it can be seen that the generation and power system are able to recover from the fault and reach the prior pre-fault steady-state solution. With the case of the longer fault duration, the generator will accelerate beyond the point where the electrical power will be less than the mechanical power and the generator will eventually become unstable. This critical clearing time can be seen in Figure 53 as the integration resulted in a $\delta_{Te}$ of 108° and is associated to a $T_{critical}$ of 0.245μs.

![Figure 53: PSpice Result of First Swing Response](image)

These results can also be seen in the hardware emulation of the generator model. Figure 54 and Figure 55 emulated fault conditions with durations of 180μs and 250μs, respectively. The results show similar behaviors for the given fault conditions for a stable and unstable case. Both of the PSpice and hardware results were qualitatively very close to the numerical integration method but quantitatively exhibited some error,
approximately less than 10% for both the critical clearing time, $T_{critical}$, and the electrical angle, $\delta_{Tc}$.

Figure 54: Hardware Results of Stable Transient Analysis

Figure 55: Hardware Results of Unstable Transient Solution
Some error is introduced through component values and tolerances but most can be contributed to the offset current of the OTA. With a zero input (zero $P_m$) an electrical angle is still present in the hardware due to the offset current flowing through the integrators and charging the capacitors. Through better designed OTAs or circuit calibration, these results can be improved.

Transient stability analysis is essential to both planning and operation of power system networks. When a fault occurs in a system, a transient reaction transpires, and when the fault is cleared, either the system returns to a stable equilibrium or the system goes unstable. This is an important area of interest in power system analysis, which could be further researched in future work.
APPENDIX C: GENERATOR CIRCUIT VALIDATION RESULTS

The lossy configuration of the generator module circuitry utilizes all of the DC Networks 1 through 4. This is accomplished by changing board jumper settings that will include the lossy network currents (from the real part of the complex network admittance), $I_1$ and $I_4$, as well as the lossless network currents $I_2$ and $I_3$ from Section 6.3.1. Again, each generator control input parameter was set to a selected fixed voltage. In addition, selected fixed load impedances are connected to all Networks 1 through 4, with $R_1 = 17.7k\Omega$, $R_2 = 17.7k\Omega$, $R_3 = 64.7k\Omega$, and $R_4 = 64.7k\Omega$.

![Figure 56: Lossy Generator Configuration Load Impedances](image)

The validation results of the lossy configuration are almost identical to the lossless configuration and the following figures following the same behavior as described in Section 6.3.1.
Figure 57: Lossy HW vs. PSpice Power Angle vs. Mechanical Input Power

Figure 58: Lossy HW and PSpice Electrical Power vs. Mechanical Input Power
Figure 59: Lossy HW and PSpice Reactive Power vs. Mechanical Input Power

Figure 60: Lossy HW and PSpice Power Angle vs. Amplifier Bias Current
Figure 61: Lossy HW and PSpice Power Angle vs. Internal Voltage Magnitude

Figure 62: Lossy HW and PSpice Electrical Power vs. Internal Voltage Magnitude
Figure 63: Lossy HW and PSpice Reactive Power vs. Internal Voltage Magnitude
## APPENDIX D: ACRONYMS AND SYMBOLS

### Table D.1: Table of Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABM</td>
<td>Analog Behavior Model</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very Large-Scale Integration</td>
</tr>
<tr>
<td>PSoC</td>
<td>Power System on a Chip</td>
</tr>
<tr>
<td>PSpice</td>
<td>PC Simulation Program with Integrated Circuit Emphasis</td>
</tr>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>OPAMP</td>
<td>Operational Amplifier</td>
</tr>
<tr>
<td>OTA</td>
<td>Operational Transconductance Amplifier</td>
</tr>
<tr>
<td>VCCS</td>
<td>Voltage-Controlled Current Source</td>
</tr>
<tr>
<td>CCVS</td>
<td>Current-Controlled Current Source</td>
</tr>
<tr>
<td>VCVS</td>
<td>Voltage-Controlled Voltage Source</td>
</tr>
<tr>
<td>SW</td>
<td>Software</td>
</tr>
<tr>
<td>HW</td>
<td>Hardware</td>
</tr>
<tr>
<td>DAQ</td>
<td>Data Acquisition</td>
</tr>
<tr>
<td>SCXI</td>
<td>Signal Conditioning Extension for Instrumentation</td>
</tr>
<tr>
<td>LabVIEW</td>
<td>Laboratory Virtual Instrumentation Engineering Workbench</td>
</tr>
<tr>
<td>GUI</td>
<td>Graphical User Interface</td>
</tr>
<tr>
<td>VAR</td>
<td>Reactive Power</td>
</tr>
<tr>
<td>PV</td>
<td>Regulated generator producing fixed real power and voltage</td>
</tr>
<tr>
<td>PQ</td>
<td>Non-Regulated generator producing constant real and reactive power</td>
</tr>
<tr>
<td>MVAR</td>
<td>Mega Volt Ampere Reactive</td>
</tr>
</tbody>
</table>
Table D.2: Table of Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>V</td>
<td>Voltage</td>
</tr>
<tr>
<td>I</td>
<td>Current</td>
</tr>
<tr>
<td>S</td>
<td>Complex Power</td>
</tr>
<tr>
<td>P</td>
<td>Real Power</td>
</tr>
<tr>
<td>Q</td>
<td>Reactive Power</td>
</tr>
<tr>
<td>C</td>
<td>Capacitance</td>
</tr>
<tr>
<td>R</td>
<td>Resistance</td>
</tr>
<tr>
<td>L</td>
<td>Inductance</td>
</tr>
<tr>
<td>Z</td>
<td>Impedance</td>
</tr>
<tr>
<td>Y</td>
<td>Admittance</td>
</tr>
<tr>
<td>$X_S$</td>
<td>Synchronous Reactance</td>
</tr>
<tr>
<td>$X'_d$</td>
<td>Direct-Axis Transient Reactance</td>
</tr>
<tr>
<td>$E_G$</td>
<td>Internal Generator Voltage</td>
</tr>
<tr>
<td>M</td>
<td>Generator Inertia Coefficient</td>
</tr>
<tr>
<td>D</td>
<td>Generator Damping Coefficient</td>
</tr>
<tr>
<td>$\delta$</td>
<td>Electrical Power Angle</td>
</tr>
<tr>
<td>$\tau$</td>
<td>Time Scale Factor</td>
</tr>
<tr>
<td>$\nu$</td>
<td>Voltage Parametric Scaling Factor</td>
</tr>
<tr>
<td>$K_p$</td>
<td>Circuit Scaling Parameter</td>
</tr>
<tr>
<td>$I_{abc}$</td>
<td>Amplifier Bias Current</td>
</tr>
<tr>
<td>$g_m$</td>
<td>Transconductance</td>
</tr>
<tr>
<td>$V_T$</td>
<td>Thermal Voltage</td>
</tr>
<tr>
<td>$G$</td>
<td>Gain</td>
</tr>
<tr>
<td>$A$</td>
<td>Maximum Current Gain</td>
</tr>
<tr>
<td>MW</td>
<td>Megawatt</td>
</tr>
<tr>
<td>MVAR</td>
<td>Mega Volt Ampere Reactive</td>
</tr>
<tr>
<td>p.u.</td>
<td>Per Unit</td>
</tr>
<tr>
<td>Deg</td>
<td>Degree</td>
</tr>
<tr>
<td>Hz</td>
<td>Hertz</td>
</tr>
</tbody>
</table>